|  |  |  |
| --- | --- | --- |
| **D**epartment of **C**omputer **E**ngineering | Subject : Computer System  Class :…ICT K56……………………  Fullname :…………………………………… Student Index:……….. | Exam ID |
|  | *Duration:* ***45 minutes*** *Date: 3/12/2014*  *Allow student to use paper documents*  *Each question has a correct option. Not decrease mark for wrong answer Should write the choice into Answer Part, others are illegal.* | 2014A |

# ANSWER PART

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Question** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** | **13** | **14** | **15** |
| **Answer** |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

# QUESTIONAIRE

**Question 1.** Consider a 256-byte cache with 8-byte blocks, an associativity of 2 and LRU block replacement. The cache is physically tagged. The processor has 32KB of physical memory. What is the number of tag bits?

(A) 8 bits (B) 9 bits (C) 10 bits (D) 11 bits

**Question 2.** Assume that there is a physical memory 64KB, the virtual memory with the length of 18 bit uses 64 bytes pages. Calculate the size of page table given that each page requires more 4 protection bits (dirty bit, valid bit, accessed bit, protection level bit), and entries must be an integral number of bytes?

(A) 8 KB (B) 4 KB (C) 2 KB (D) 1 KB

**Question 3.** For a data cache with a 85% hit rate and a 2-cycle hit latency, calculate the average memory access latency. Assume that latency to memory and the cache miss penalty together is 120 cycles. Note: The

cache must be accessed after memory returns the data.

(A) 22.0 cycles (B) 18.5 cycles (C) 20.00 cycles (D) 11.92 cycles

**Question 4.** A computer is designed to enable 6-stages pipeline control so that each instruction can be completed in 6 cycles. How many cycles are needed to completely execute a software has 20 instructions? Here, all instructions can be executed without being stopped halfway.

(A) 20 (B) 21 (C) 24 (D) 25

**Question 5.** Pipeline hazard issues occur at some lines in the source code below. Which of the following warning is wrong?

|  |  |  |
| --- | --- | --- |
|  | .set noreorder | (A) Data Hazard between line 2-3 |
| *1* | li t1, 2012 // assign |  |
| *2* | lw t2, 4(t1) // load from memory | (B) Control Hazard between line 4 |
| *3* | lw t3, 0(t2) // load from memory |  |
| *4* | beq t1,t3, skip // compare | (C) Data Hazard at line 3-4 |
| *5* | sw t2, 0(t1) // store into memory |  |
| *6* | skip: and t3,t1,t2 // simple operation | (D) Data Hazard at line 5-6 |

**Question 6.** Which of the following is superscalar architecture?

1. (B)

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

(C) (D)

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

IF

ID

EX

MEM

WB

**Question 7.** Which hazard does Forwading method resolve?

(A) Data Hazard (B) Structure Hazard (C) Control Hazard (D) Data & Structure Hazard

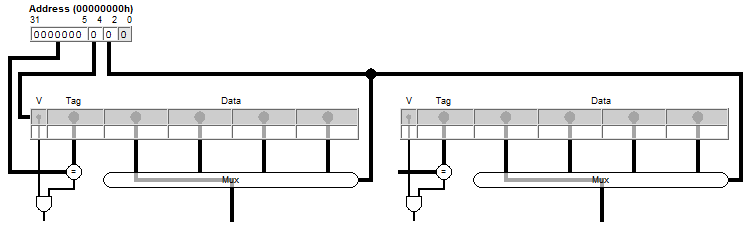
**Question 8.** Where is the Translation Look-Aside Buffer module?

(A) Cache Memory (B) CPU (C) Main Memory (D) Hard disk

**Question 9.** Which kind of cache is the most appropriate with the below figure?

(A) 2-way 4 blocks cache (B) 4-way 8 blocks cache

(C) direct mapped cache (D) full associative cache



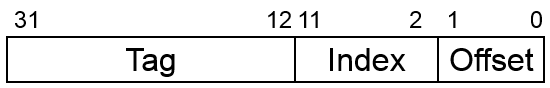
**Question 10.** A DRAM with 8-bank interleaved memory. The width of each bank is 1 byte. Bus width is 32 bit. The latency for address transfer is 3 cycles, for DRAM access is 20 cycles, and for data transfer from DRAM to cache is 3 cycles. How many cycles is taken for tranfer a 16-byte block?

(A) 48 (B) 55 (C) 58 (D) 59

**Question 11.** A DRAM with 4-bank interleaved memory. Bus width is 32 bit. Miss rate = 4%. Which bank does the address 0x823FAC belong to?

(A) 0 (B) 1 (C) 2 (D) 3

**Question 12**. The meaning of address bits as figure below. Here, cache is direct mapped. How large is the block size?



(A) 4KB (B) 2KB (C) 12 byte (D) 16 byte

**Question 13**. The table following is TLB. Describe the status of address 0xB4FB: hit/miss/unknown? on disk/on physical mem? if in mem, what is the physical address?

20 bits

12 bit

*Virtual Address*

|  |  |  |
| --- | --- | --- |
| Valid bit | Tag | Physical Page Number |
| 1 | 11 | 12 |
| 0 | 7 | 4 |
| 1 | 3 | 6 |
| 0 | 4 | 9 |

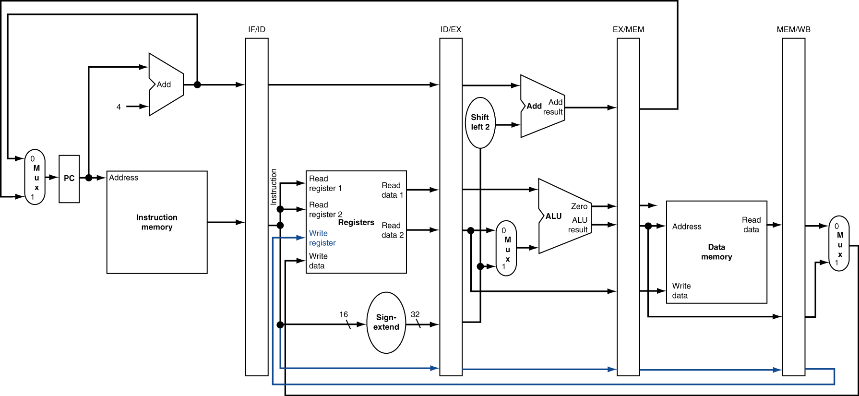
**Question 14.** In the pipeline figure below, the pipeline has 5 instructions with format op rd, rs1, rs2

At **ID stage**, which register is Read Register 1?

(A) $8 (B) $11 (C) $5 (D) $14

**Question 15**. In the pipeline figure below, at **ID stage**, which register is Write Register?

(A) $4 (B) $15 (C) $10 (D) $13

add $1, $2, $3 sub $4, $5, $6 xor $7, $8, $9 xor $10, $11, $12 and$13, $14, $15

**Question 1**. Consider a 256-byte cache with 8-byte blocks, an associativity of 2 and LRU block replacement. The cache is physically tagged. The processor has 32KB of physical memory. What is the number of tag bits?



**Question 2.** Assume that there is a physical memory 64KB, the virtual memory with the length of 18 bit uses 64 bytes pages. Calculate the size of page table given that each page requires more 4 protection bits (dirty bit, valid bit, accessed bit, protection level bit), and entries must be an integral number of bytes?

****

**Question 3.** For a data cache with a 85% hit rate and a 2-cycle hit latency, calculate the average memory access latency. Assume that latency to memory and the cache miss penalty together is 120 cycles. Note: The

cache must be accessed after memory returns the data.



**Question 4.** A computer is designed to enable 6-stages pipeline control so that each instruction can be completed in 6 cycles. How many cycles are needed to completely execute a software has 20 instructions ? Here, all instructions can be executed without being stopped halfway.



x

**Question 10.** A DRAM with 8-bank interleaved memory. The width of each bank is 1 byte. Bus width is 32 bit. The latency for address transfer is 3 cycles, for DRAM access is 20 cycles, and for data transfer from DRAM to cache is 3 cycles. How many cycles is taken for transfer a 16-byte block?

